Technical description Video Amplifier R762746

Video Amplifier

The video signal arrives at pin 2 of J1 and is terminated into 75Ω the resistors R1...6. The first half of IC2 switches the base of Q2 between this video signal (no ABL-Automatic Black Level) and the reference voltage on pin 1 of IC10 (during ABL).

Via buffer Q1 and D3, the signal is fed to the input of a non-inverting amplifier formed by Q2 and Q3. The diode D3 serves as protection for Q1 against high inverse Vbe voltage during blanking. The resistors R13, R14 form together with R15 and R104 a divider that is chosen to limit the voltage at the emitter of the transistor Q1 during overdrive conditions of the input. This prevents saturation of the amplifier.

The amplified signal arrives at pin 4 of the VPH08. Feedback for the previous amplifier is taken from pin 3 of the VPH08. The potentiometer P1 determines the GAIN and C1/R21 improve the frequency response.
IC1 (VPH08) is a cascode class A amplifier with built in buffer stage and external load resistor, formed by R32...35.
Via pin 2 of J3 and J4, the signal goes to the IBCL (Individual Beam Current Limiting) and ABL measurements stages and finally arrives at the cathode of the CRT. The components D4..D7,C49, R103, D28, B1, B2 and R95 protect the amplifier against arcing.

IBCL measurement

With the transistor Q4, the mean cathode current is measured. The current flows via D12, D13 and Q5 and through Q4 to R45. There, the current is converted into a voltage and is sent to the RGB driver module. The capacitor C10 prevents high frequency currents to flow through Q4. The resistor R46 and zener Z4 form a protection network.

Switch

ABL measurement+

During the non-ABL period, the base-emitter junction of the transistor Q6 is shorted by the transistor Q5. The cathode current flows through R51 and Q5 to the IBCL measurement stage. If the cathode current is high, the voltage drop across the resistor R51 increases and D12/D13 also come into conduction. The gate of Q5 is held at +5.6V with Z1 and R49/R50.
During the ABL interval, the optocoupler IC7 comes into conduction and shorts the gate-source of Q5. Now the cathode current can flow through the transistor Q6, R52 and R53 to the ABL control loop. By shorting the transistor Q6 outside the ABL interval, smearing is prevented.
The optocoupler is controlled by the circuit around the transistors Q10 and Q11. During the blanking, the BL-signal (Blanking) is negative (-15V). The pulse is integrated by R80/C22. During the blanking, the BL-signal is wide enough to get Q10, Q11 and IC7 into conduction until some time after the vertical blanking.

ABL Control Loop

This circuit has to keep the cathode current just above the black level constant. The ABL measurement is performed at the end of the vertical flyback, when the electon beam is moved outside the phosphor screen of the CRT in order not to see these measurements lines.
The ABL interval is initiated by a 12V pulse of 20μs, which is AC coupled on the IBCL line. The pulse is coupled via R54 and C13 to the base of Q7. The resistor R55 keeps the diode D15 into conduction if there is no pulse to prevent false triggering. The pulse at the emitter of Q7 and MP7 is used to perform the leakage current measurement and is now called leakage pulse. With the trailing edge of this pulse, the transistor Q8 starts to conduct through the network C14, R59 and R60 for about 20μs. This pulse at MP6 is now called the measurement pulse. The total ABL interval is 40μs wide and

is electrically formed by D17, D18 on R61 and C15.
This pulse is used to inhibit the blanking and to switch Q1 to the reference voltage. This voltage is formed by R78 and R79 during the measurement pulse and is then +2.4V.

During the leakage measurement is transistor Q16 in conduction and lowers this reference with R101 to +2.0V. IC10 buffers this voltage and can sink the base current of Q1.
The leakage current enters the control loop through pin 10 ofJ3/J4 and is converted to a voltage with R71. This voltage is first amplified with IC9 pins 1, 2 and 3 with a factor 90. The diodes D22 and D23 limit the input levels.

During the leakage measurement the emitter of the transistor Q7 is high and pins 1, 10 of the switch IC4 are closed. The amplified voltage comes on C18 and is compared with ground by IC9, pins 5, 6 and 7 which adjusts the bottom of R71 until steady state. This system compensates for leakage currents that might flow out of the cathode.

During the measurement pulse is the level at MP6 high and the switch IC4 pin 3, 4 and 9 is closed. The input reference is now 2.4V at the base of the transistor Q1 and this should give a cathode current of about 20μs.

The amplified voltage that corresponds to this current comes on capacitor C19 and is buffered by IC3 pin 5, 6 and 7. The voltage is compared by IC3 pin 1, 2 and 3 with a reference and adjusts the output DC level at the collector of Q3 trough R30.

During the leakage measurement the input voltage at Q1 is equal to 2V, and the output voltage should be 185V. This voltage is divided with R68, R69, R70 and P30 to 0V. This voltage is buffered by IC6 pins 5, 6, 7, and compared by the comparators IC5 with 2 references. The potentiometer P30 is aligned so that the LED D30 is turned off at an output black level of +185V. The G2 potentiometers can then easily be adjusted

(if the LED D30 turns off, the G2 is at the correct level because the cathode is at 185V black level.

Regulated Power Supply

The Power Supply had to be regulated to guarantee the performance of the VPH08 and to eliminate variations on the +210V Power Supply. The +200V is divided by R90, R91, R92 and P3 to 0V and compared with ground by IC6 pins 1, 2 and 3. If the output voltage is too low, pin 1 goes higher and more current is flowing through Q15, Q13 and Q14 as to raise the output until steady state. The transistor Q12 limits the peak current.